WHAT IS CLAIMED IS:

1. An OLED panel driving apparatus having an OLED in each intersecting point of a plurality of common anode lines and a plurality of common cathode lines, which are aligned in a matrix configuration, to form a pixel, the OLED panel driving apparatus further comprising:

a data driving circuit connected to a plurality of common anode lines, and having a plurality of data output unit selectively connecting each of the common anode lines to a constant current source or a high impedance terminal HIZ; and

a scan driving circuit connected to the plurality of common cathode lines, and having a plurality of scan output units selectively connecting each of the common cathode lines at least to a high impedance terminal HIZ or a grounding earth.

2. The OLED panel driving apparatus according to claim 1, wherein the scan output unit further comprises a high voltage terminal to selectively connect each of the common cathode lines to the high voltage terminal, the high impedance terminal HIZ or the grounding earth.

3. The OLED panel driving apparatus according to claim 2, further comprising an OLED control circuit for generating various signals including a horizontal synchronization signal, a vertical synchronization signal and a display data signal.

4. The OLED panel driving apparatus according to claim 3, wherein the scan

driving circuit comprises:

a scan output unit;

a shift register unit for generating a scan control signal C_{SCAN} with respect to the common cathode line; and

a control logic unit for executing the logic processing of the scan control signal C_{SCAN} supplied from the shift register unit in order to generate a high impedance control signal C_{HIZ}, and to supply to the scan output unit.

5. The OLED panel driving apparatus according to claim 4, wherein the scan output unit comprises:

an inverter gate, its input end being connected to the high impedance control signal end C_{HIZ};

a NOR gate, its one input end being connected to the scan control signal end C_{SCAN}, and its the other input end being connected to the high impedance control signal end C_{HIZ};

a NAND gate, its one input end being connected to the scan control signal end C_{SCAN}, and its the other input end being connected to the output end of the inverter gate;

a first level shifter being connected to the output end of the NAND gate and converting logic level into the high voltage level;

a second level shifter being connected to the output end of the NOR gate and converting logic level into the high voltage level;

a first PMOSFET having a gate connected to the first level shift and a source connected to the high voltage terminal; and

a first NMOSFET having a gate connected to the second level shift, a drain

connected to the drain of the first PMOSFET, and a source being grounded, wherein

the common cathode lines are connected to the first PMOSFET and the drain of the first NMOSFET.

6. The OLED panel driving apparatus according to claim 4, wherein the shift register unit is configured to have shift registers as many as the number of the common cathode lines;

the vertical synchronization signal is applied to data input end of a first row of a shift register in the shift registers;

the horizontal synchronization signal is applied to the all clock ends of the shift register; and

the output of one row of the shift registers is connected to a corresponding row of a scan control signal end C_{SCAN} in the scan output unit, and to a data input end of a next row of the shift register.

7. The OLED panel driving apparatus according to claim 6, wherein

the control logic unit is configured to have 2-input XNOR gates as many as the number of the common cathode lines;

one input end of each of the XNOR gates is connected to the output end of its corresponding row of the shift register;

the other input end of each of the XNOR gates is connected to the output end of a next row of the shift register; and

the output end is connected to the high impedance control signal end C_{HIZ} of its corresponding row of the scan output unit.

8. The OLED panel driving apparatus according to claim 3, wherein the data driving circuit comprises:

a data output unit;

a shift register/latch unit for sequentially shifting and storing the data applied to the common anode line in accordance with the control signal from the OLED control circuit; and

a PWM generating unit for converting the data supplied from the shift register/latch unit into a control signal PWM having various time width in accordance with gray level of the data, and supplying to the data output unit.

9. The OLED panel driving apparatus according to claim 8, wherein the data output unit comprises:

a second PMOSFET and a third PMOSFET to form current mirror circuits;

a third level shifter for converting the logic level of the control signal PWM supplied from the PWM generating unit into the high voltage level; and

a fourth PMOSFET for selectively connecting the common anode line to the constant current source and the high impedance terminal HIZ with "on"/"off" by the third level shifter.

10. The OLED panel driving apparatus according to claim 9, further comprising a second NMOSFET for grounding the common anode line with "on" by an outer control signal Reset in the "off" state of the fourth PMOSFET.

11. A method of driving an OLED panel having an OLED in each intersecting point of a plurality of common anode lines and a plurality of common

cathode lines, which are aligned in a matrix configuration, to form a pixel, the method including the step of maintaining, in a high impedance state, the common cathode lines in the rest of the rows except one row of the currently scanned common cathode line while being sequentially scanned after converted into grounding level GND in the process of applying constant current to the common anode lines by a control signal PWM having various time width in accordance with gray level of displayed pixel data.

12. The method of driving an OLED panel according to claim 11, wherein the row of the common cathode line right prior to the row of the currently scanned common cathode line is connected to a high voltage terminal.